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KITOV, ZEEV	
ART UNIT	**PAPER NUMBER**
2836	

DATE MAILED: 10/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/808,676	COMEAU, ALAIN R.	
	Examiner	Art Unit	
	Zeev Kitov	2836	

-- The MAILING DATE of this communication appears on the cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1- 5, 7 - 14,16 - 24* is/are rejected.

7)☒ Claim(s) *6, 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 March 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Examiner acknowledges a submission of the amendment and arguments filed on June 11, 2003. Claims 1, 4, 9, 13 and 24 are amended. Amendment and arguments have overcome objection to Claims 1, 9, 4, 13 and 24. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. The new rejection follows.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claims 6 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Following statements make the claims indefinite: "the resulting leakage current from said source voltage is approximately 10^{-14} A/μm". The current is defined as amount of charge per cross sectional area (per squared value of length). Citation of current value in amperes per units of length makes the claims indefinite. Accordingly metes and bounds of the claim cannot be determined. The claim has not been treated with regard to prior art.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 5 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Smith (US 5,903,419). Smith discloses an ESD protection having a transistor with gate, source, drain and substrate terminals (element 204 in Fig. 2), an input terminal coupled to the source terminal of the transistor (I/O PAD 14 in Fig. 2), a reference point coupled to the gate and substrate terminals of the transistor (Vdd in Fig. 2), and an output signal terminal coupled to the drain terminal of the transistor (base of transistor 202 is coupled to the drain of transistor 204 in Fig. 2). Due to a diode (element 206 in Fig. 2), a gate to substrate voltage is always positive, which moves the PMOS transistor into sub-threshold regime. Increase of the transistor source voltage reduces the source-to-gate threshold. One of the goals of the invention in the reference is a reduction of a leak current (col. 2, lines 20 – 29, col. 4, lines 1 –5, col. 9, lines 25 –35). The Smith structure inherently reduces the leakage current to a sub-threshold level.

Regarding Claim 5, Smith discloses the device having the source voltage of a few hundreds millivolts (a voltage drop across diode 206 in Fig. 2).

Regarding Claim 8, discloses a PMOS transistor (element 204 in Fig. 2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 7 and 2 - 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith in a view of A. Sedra and K. Smith textbook "Microelectronic Circuits". As was stated above, Smith discloses all the elements of Claim 1. However, regarding Claim 7, it does not disclose the NMOS transistor. According to the Microelectronic Circuits textbook (pages 3442 -343), the NMOS and PMOS transistors are equivalents and are interchangeable. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used NMOS transistor as equivalent replacement for PMOS transistor, because as the textbook states (pages 243 -343), they are equivalents and interchangeable. Selection of particular type of transistor is a designer decision, which is far from being an inventive step.

Regarding Claims 2 - 4, Smith discloses the reference point (element Vdd in Fig. 2), which for PMOS transistor plays the same role as the ground, or Vss (the lowest potential) voltage for NMOS transistor. Therefore, for the equivalent PMOS transistor the reference potential is equal Vdd volts, rather than 0 volts. As to the reference point equal 0 or Vss volts, reducing amount of diodes in a string of diodes (element 200 in Fig.2) to one creates the reference equal 0 volts and shorting a gate diode (element 206 in Fig. 2) together with a whole string of diodes (element 200 in Fig. 2) makes the

reference equal Vss for NMOS transistor (or Vdd for PMOS transistor). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Smith circuit by changing amount of diodes in the string and shorting the gate diode, because it is well known in the art and common way of changing the transistor reference.

5. Claims 9, 11 – 14, 18 and 22 – 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watt et al. (US 5,751,507) a view of Smith.

Regarding Claims 9 and 18, Watt et al. discloses an ESD protection solution for a plurality of low operating voltage devices having a plurality of input terminals (input pads 1, 2, ..., N in Fig. 2). Each input has its own ESD protection (elements D1 and D3 in Fig. 2).

However, he does not disclose a low leakage current solution for ESD protection devices. Smith discloses an ESD protection having a transistor with gate, source, drain and substrate terminals (element 204 in Fig. 2), an input terminal coupled to the source terminal of the transistor (I/O PAD 14 in Fig. 2), a reference point coupled to the gate and substrate terminals of the transistor (Vdd in Fig. 2), and an output signal terminal coupled to the drain terminal of the transistor (base of transistor 202 is coupled to the drain of transistor 204 in Fig. 2). Due to a diode (element 206 in Fig. 2), a gate to substrate voltage is always positive, which moves the PMOS transistor into sub-threshold regime. Increase of the transistor source voltage reduces the source-to-gate threshold. One of the goals of the invention in the reference is a reduction of a leak current (col. 2, lines 20 – 29, col. 4, lines 1 –5, col. 9, lines 25 –35). Both patents have

the same problem solving area, namely providing an efficient ESD protection for integrated circuits. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the plurality of transistors according to Smith protecting each of the inputs of the Watt et al. circuit, because as well known in the art and stressed by Smith (col. 2, lines 20 – 29), the leakage current presents a problem in many electronic circuits, especially in a view that they increase with a temperature.

Regarding Claim 14, Smith discloses the device having the source voltage of a few hundreds millivolts (a voltage drop across diode 206 in Fig. 2). A motivation for combining the references is the same as above.

6. Claims 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watt et al. in view of Smith and further in a view of Ker et al. article "Capacitor-Coupled ESD Protection Circuit for Deep-Submicron Low-Voltage CMOS ASIC". As was stated above, Watt et al. and Smith disclose all the elements of Claim 9. However, regarding Claim 10. However, regarding Claim10, they do not disclose the solution according to teachings of Watt et al. and Smith being used for protection of the low voltage CMOS circuit. Ker et al. discloses an ESD protection for the low voltage CMOS circuit. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the solution according to teachings of Watt et al. and Smith for protection of the low voltage CMOS circuit, because as Ker et al. state (see Operating Principles pages 310 – 311), the submicron low voltage CMOS circuits more

than other circuits need the ESD protection. Additionally, as well known in the art, the modern digital IC's widely use low voltage supplies. Since the trigger voltage of the ESD circuit is usually set slightly higher than the supply voltage, there is variety of problems associated with the ESD protection of the low voltage supplied circuits.

7. Claims 11 – 13, 16, 19, 17, 20 and 22 – 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watt et al. in a view of Smith and further in a view of A. Sedra and K. Smith textbook "Microelectronic Circuits". As was stated above, Watt et al. and Smith disclose all the elements of Claim 9. However, regarding Claims 16 and 19, they do not disclose the NMOS transistor. According to the Microelectronic Circuits textbook (pages 3442 -343), the NMOS and PMOS transistors are equivalents and are interchangeable. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used NMOS transistor as equivalent replacement for PMOS transistor, because as the textbook states (pages 243 -343), they are equivalents and interchangeable. Selection of particular type of transistor is a designer decision, which is far from being an inventive step.

Regarding Claim 17 and 20, Smith discloses a PMOS transistor (element 204 in Fig. 2). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the NMOS transistor of Watt by PMOS transistor according to Smith, because as well known in the art, both transistors are functionally identical with exception of their polarities and thus mutually replaceable with minor adjustments in the associated circuit due to a change of polarity.

Regarding Claims 11 – 13 and 22 - 24, Smith discloses the reference point (element Vdd in Fig. 2), which for PMOS transistor plays the same role as the ground, or Vss (the lowest potential) voltage for NMOS transistor. Therefore, for the equivalent PMOS transistor the reference potential is equal Vdd volts, rather than 0 volts. As to the reference point equal 0 or Vss volts, reducing amount of diodes in a string of diodes (element 200 in Fig.2) to one creates the reference equal 0 volts and shorting a gate diode (element 206 in Fig. 2) together with a whole string of diodes (element 200 in Fig. 2) makes the reference equal Vss for NMOS transistor (or Vdd for PMOS transistor). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Smith circuit by changing amount of diodes in the string and shorting the gate diode, because it is well known in the art and common way of changing the transistor reference.

Allowable Subject Matter

Claims 6 and 15 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. A reason for that is that Applicant disclosed in the Specification criticality of achieving particularly low leakage current values.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Response to Arguments

In his arguments to rejection of Claims 6 and 15 under 112, 2nd paragraph, the Applicant traverses Examiner's reasoning stating that "Claims 6and 15 are structured to address different protection levels (as determined by different width) by normalizing the leakage on per unit width basis". And further, "as such, the reference to 10^{-14} A/μm in the Claims 6 and 15 are definite and would be understood by those skilled in the art". Applicant further gives alternative formulation of the current density stating a width. So the width is assumed by applicant but for some reason is not used. That leaves Claims 6 and 15 indefinite.

An Applicant's Arguments regarding Claim 1 and 9 rejections devoted to critique of deficiencies of the Smith reference is missing the point. The Smith reference discloses all the elements of the claims, thus satisfying the requirements.

a) Regarding Applicant's Arguments on Claims 1 and 9 rejections.

The Applicant's statement that "the reverse bias in Smith circuit is possible if current is already flowing through PMOS transistor 204 (of Smith) and through diodes 200 (of Smith)" (page 9, lines 16 – 17), one must say that the leakage currents always flow through the parts including diodes thus forming a voltage drop across them, while the gate of transistor is connected directly to the Vdd. Therefore, the reverse bias is definitely formed in regular conditions without the ESD event.

As to Applicant's arguments (pages 9 - 10 of Arguments) that the Smith reference fails to show certain features upon which Applicant relies (i.e. higher level of performance, lower requirements to the parts quality, technological advantages in CMOS realization and lower degree of complexity) are not recited in the rejected claims. Although the claims are interpreted in light of the Specification, limitations from the Specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

b) Regarding Applicant's Arguments on Claims 9, 14, 17, 18 and 20 rejections.

With respect to the Applicant's argument, that neither of the references suggests to combine the references, (i) as was stated in the Office Action, Smith recites a problem of leakage currents and their rise with the temperature (col. 2, lines 20 – 23). (ii) The problem of leakage currents is well known in the art, especially for devices with limited

power supplies, such as a battery supply. Therefore, no hindsight is necessary to appreciate the leakage currents problem.

Regarding Claim 14 rejection the Applicant alleges that the Architecture and objectives of the Smith invention are different from that of the Applicant (page 16, line 15). As was stated above, the Smith reference satisfies all the limitations of Claim 1. As to recited Applicant's different purpose, it has been held that recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations *Ex parte Masham*, 2 USPQ2d 1647 (1987).

Further regarding Claim 14, an example of comparison of the Office Action statement with the claim limitation provided by the Applicant shows that they are identical, because "a few hundreds millivolts" of the Office Action is the same as "a few 100 mV" of the claim, seepage 16 of the Arguments).

Regarding Claims 17 and 20, the Arguments are moot in a view of new version of the claim rejection.

Regarding Applicant's allegation that the Claim 10 rejection does not provide the motivation to combine the references of Ker and Smith, Examiner should draw the Applicant attention to the Claim 10 rejection in the Office Action, which includes a proper motivation. As to Applicant's argument that the Ker circuit is different from that of the Applicant, it has been held that the test for obviousness is not whether the features of one reference may be bodily incorporated into the other to produce the claimed

subject matter but simply what the combination of references makes obvious to one of ordinary skill in the pertinent art. *In re Bozek*, 163, USPQ 545 (CCPA 1969).

As to Applicant's Arguments with respect to Claims 16 and 19 rejections, they recite the same allegation that the Smith reference is not valid rejection for Claims 1, 5 and 8, which was addressed above.

Arguments regarding claims 11 – 13 and 22 – 24 rejection are moot in a view of reformulated rejections.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose telephone number is (703) 305-0759. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (703) 308-3119. The fax phone number for organization where this application or proceedings is assigned is (703) 972-9306 for all communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Z.K.
09/29/2003

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